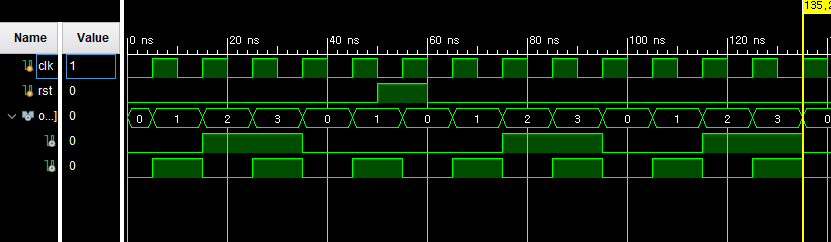
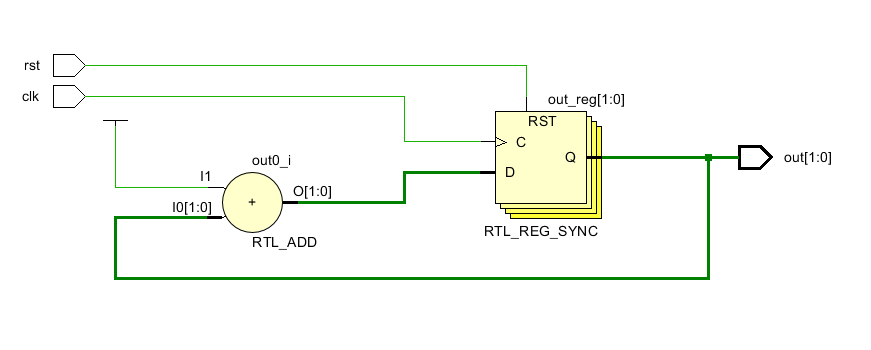
2bit counter

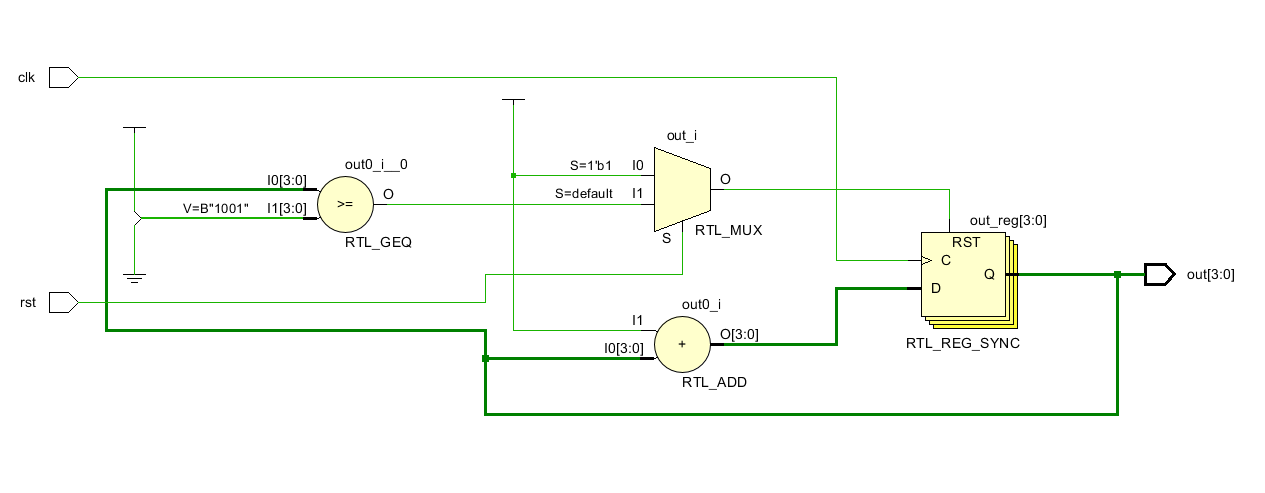
Table X

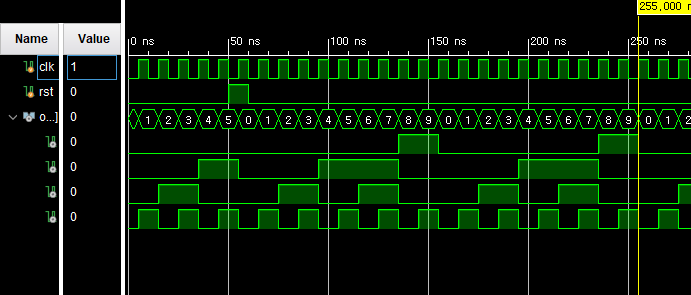




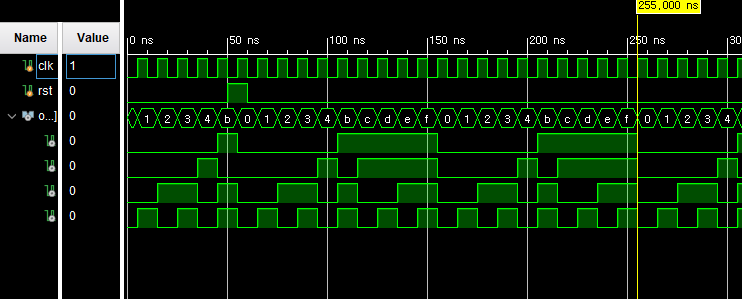
Decade counter

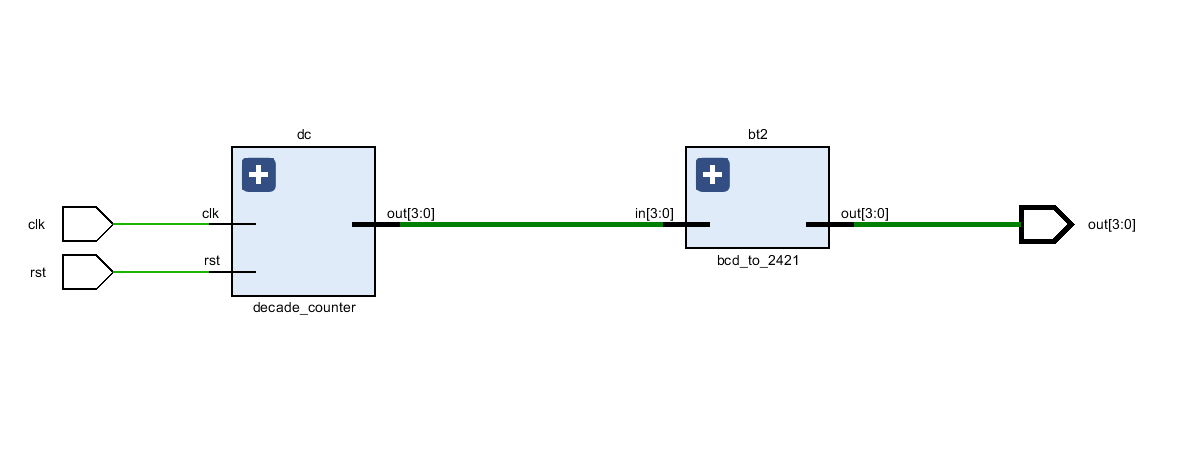
0~9 (4bit)

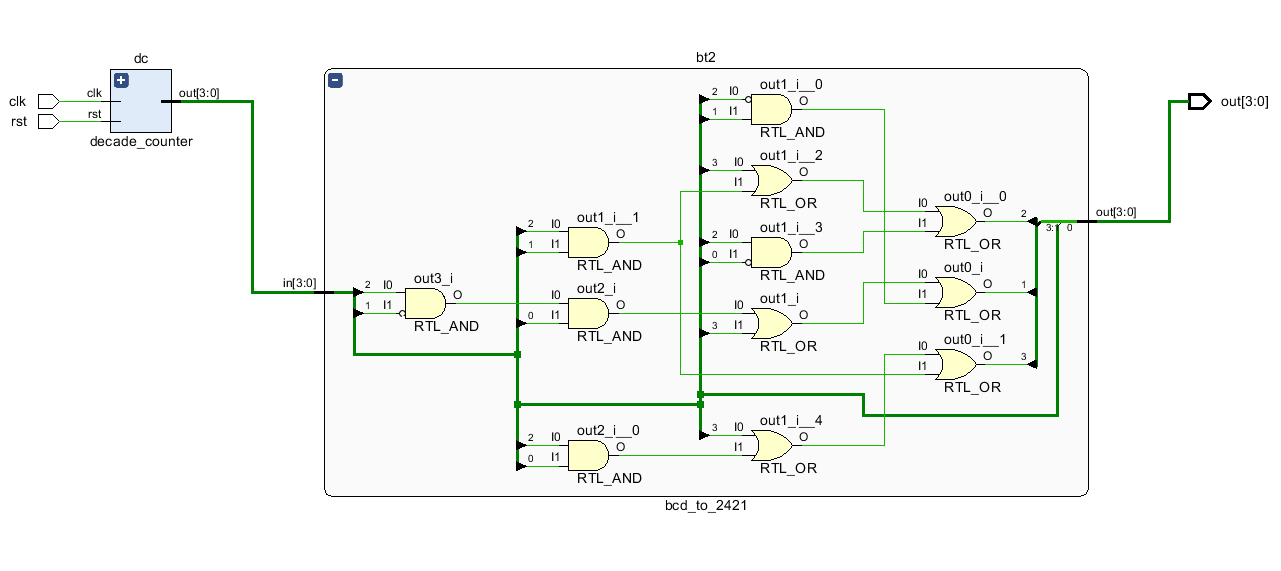




4bit 2421 decade counter







`timescale 1ns / 1ps

module two\_bit\_counter(

clk, rst, out

);

input clk, rst;

output[1:0] out;

reg[1:0] out;

initial out = 2'b00;

always @(posedge clk) begin

if(rst) begin

out <= 2'b00;

end

else begin

out <= out + 1;

end

end

endmodule

module decade\_counter(

clk, rst, out

);

input clk, rst;

output[3:0] out;

reg[3:0] out;

initial out = 4'b0000;

always @(posedge clk) begin

if(rst) begin

out <= 4'b0000;

end

else if(out >= 4'b1001) begin

out <= 4'b0000;

end

else begin

out <= out + 1;

end

end

endmodule

module bcd\_to\_2421(

in, out

);

input[3:0] in;

output[3:0] out;

assign out[3] = in[3]|(in[2]&in[0])|(in[2]&in[1]);

assign out[2] = in[3]|(in[2]&in[1])|(in[2]&~in[0]);

assign out[1] = (in[2]&~in[1]&in[0])|in[3]|(~in[2]&in[1]);

assign out[0] = in[0];

endmodule

module code2421\_counter(

clk, rst, out

);

input clk, rst;

output[3:0] out;

wire[3:0] connecter;

decade\_counter dc(

.clk(clk),

.rst(rst),

.out(connecter)

);

bcd\_to\_2421 bt2(

.in(connecter),

.out(out)

);

Endmodule

`timescale 1ns / 1ps

module twobit\_sim;

reg clk, rst;

wire[1:0] out;

two\_bit\_counter tbc(

.clk(clk),

.rst(rst),

.out(out)

);

initial clk = 0;

initial rst = 0;

always clk = #5 clk + 1;

initial begin

#50

assign rst = ~rst;

#10

assign rst = ~rst;

#1600

$finish;

end

endmodule

module decade\_sim;

reg clk, rst;

wire[3:0] out;

decade\_counter dc(

.clk(clk),

.rst(rst),

.out(out)

);

initial clk = 0;

initial rst = 0;

always clk = #5 clk + 1;

initial begin

#50

assign rst = ~rst;

#10

assign rst = ~rst;

#1600

$finish;

end

endmodule

module code2421\_sim;

reg clk, rst;

wire[3:0] out;

code2421\_counter cc(

.clk(clk),

.rst(rst),

.out(out)

);

initial clk = 0;

initial rst = 0;

always clk = #5 clk + 1;

initial begin

#50

assign rst = ~rst;

#10

assign rst = ~rst;

#1600

$finish;

end

endmodule